Course Syllabus

| 1. | Course title | Logic Design |
|-----|--|--------------------------------|
| 2. | Course number | 1901204 |
| 3. | Credit hours (theory, practical) | 3 |
| | Contact hours (theory, practical) | 3 |
| 4. | Prerequisites/corequisites | Discrete Mathematics (1901101) |
| 5. | Program title | B.Sc. in Computer Science |
| 6. | Year of study and semester (s) | |
| 7. | Final Qualification | |
| 8. | Other department (s) involved in teaching the course | N/A |
| 9. | Language of Instruction | English |
| 10. | Date of production/revision | |
| 11. | Required/ Elective | Required |

12. Course Coordinator:

مركـز الاعنما وضمان الجود

13. Other instructors:

14. Course Description:

Main concepts of Logic Design; Boolean Algebra; Basic Definitions; Basic Theorems and Properties; Boolean Functions; Canonical and Standard Forms; Digital Logic Gates; Minimization Methods; Combinational Logic; Sequential Logic. Numbering Systems; Binary Codes; Boolean Algebra; Gate-Level Minimization; Algebraic Simplifications; Karnaugh Maps; Don't-Care conditions; NAND and NOR Implementation; Combinational Logic; Adders and subtractors; Decoders and Encoders; Multiplexers and Demultiplexors; ROMS and PLAs; Sequential Logic; Flip Flops; Registers, Counters, and Serial adder.





15. Course aims and outcomes:

A- Aims:

The main goal of this course is to equip students with required mathematical knowledge to analyze and design a logical circuit.

B- Intended Learning Outcomes (ILOs): Upon successful completion of this course students will be able to ...

A. Knowledge and Understanding: Students should ...

A1) Understand the Boolean algebra theorems and properties.

A2) Understand the main concepts of gate-level minimization.

A3) Understand the combinational logical circuits.

A4) Understand the sequential logical circuits.

B. Intellectual skills: with the ability to ...

B1) Simplify Boolean Functions using Boolean algebra identities

B2) Simplify Boolean Functions using K-map

B3) Convert Boolean functions into standard and canonical forms

B4) Link truth table, Boolean functions and circuit diagrams together.

B5) Analyze Problems and Design circuits.

C. Subject specific skills – with ability to ...

C1) Designing of combinational circuits.

C2) Designing of sequential circuits

D. Transferable skills – with ability to

D1) Discuss and work in a group in order to design the main logic circuits.

D2) Discuss and work in a group in order to design and implement assigned combinational and sequential circuits.

D3) Use tools to design and analyze circuits.

| 16. Topic Outline and Schedule: |
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| Торіс | Week | ILOs | Program SOs ¹ | TLA (teaching, learning and Assessment) |
|---|------|---------------------|--------------------------|---|
| Introduction | 1 | | | CH 1 |
| Boolean Algebra: operators of Boolean Algebra, Boolean functions (truth table, implementation of Boolean functions). | 1 | A1, A2, B1 A | а | Sections 2.1 - 2.3, 2.5 Quiz, Midterm, Final |
| Boolean Algebra: Simplification and complement | 2 | A1, A2, B3 A, B1 | a | Sections 2.4, 2.5 Quiz, Midterm, Final |
| Boolean Algebra: Standard Forms (Sum of Products, and Product of | 2 | A1, B3 A, B1 | a, j | Section 2.6 Quiz, Midterm, Final |

¹ The ABET outcomes

| Sums) | | | | |
|--|-------|---|------------|---|
| Quiz 1 Boolean Algebra: Canonical Forms (sum of minterms, and product of maxterms) K-Map: 2- variables, 3- variables, 4- variables. | 2,3 | A1,A2, B2, B3, B4 A, B1 | a | Sections 2.6, 3.1-3.3 Quiz, Midterm, Final |
| K-Map: Product of sum simplification, Do not care conditions NAND and NOR Implementation Quiz 2 | 3 | A1,A2, B2,B4 A, B1 | a, i, j | Sections 3.4 - 3.6 Midterm, Final |
| Midterm exam | 3 | | | |
| Combinational Circuits: Analysis and Design Binary Adder | 4 | A2,A3, B2, B3, B4, B5, C1, D1, D2, D3 A, B1, C2 | b, c, i, j | Sections 4.1 - 4.5 Quiz, Final |
| Binary Subtractor and Multiplication Quiz 3 | 4 | A3, B5, C1, D2, D3 A, B1, C2 | b, c, i | Sections 4.5, 4.7 Quiz, Final |
| Decimal Adder Comparator | 4 | A3, B5, C1, D1, D2, D3 A, B1, C2 | b, c, i | Sections 4.6-4.8 Quiz, Final |
| Decoder Encoder Multiplexers Demultiplexers ROM | 4 9/4 | A3, C1, B5, D1, D3 A, B1, C2 | b, i | Sections 4.9, 4.10, 4.11, 7.5 Quiz, Final |
| Quiz 4 Flip-Flop Analyzing Sequential Circuit | 5 | A4, B2, C2, D2, D3 A, B1, C2 | b, i | Sections 5.1-5.5 Quiz, Final |
| Design Sequential Circuit, | 5 | A4, B2, B5, C2, D2, D3 A, B1, C2 b | C, i, j | Section 5.8 Final |
| Registers Serial adders Counter | 5 | A4, B5, C2, D1, D2, D3 A, B1, C2 | b, i | Sections 6.1 - 6.3 Final |
| Review | 5 | | | |
| Final | 6 | | | |

(Please mention instructors per topic if the course topics are being taught by more than one instructor)

17. Evaluation Methods and Course Requirements (Optional):

Opportunities to demonstrate achievement of the ILOs are provided through the following <u>assessment</u> <u>methods and requirements</u>:

There will be several assessment methods of evaluation the performance of the students such as, grading the quizzes; practical quizzes; conducting the Midterm and the Final Exams

18. Course Policies:

A- Attendance policies:

Deliberate abstention from attending 1901204 classes and any other similar acts will lead to student deprivation from the course according to the UJ regulations

B- Absences from exams and handing in assignments on time:

If you miss the midterm, then a makeup exam will not be provided unless you submit a valid absence excuse, within three days from the midterm, to your lecturer. This excuse must be signed and stamped from the UJ hospital in order to be valid. If your lecturer accepts the excuse then you will be able to take the midterm makeup. You need to follow up the departmental announcements regarding the makeup date and time. Please note that the lecturer may either accept or reject your excuse based on UJ regulations

C- Health and safety procedures:

N/A

D- Honesty policy regarding cheating, plagiarism, misbehavior:

All students in this course must read the University policies on plagiarism and academic honesty

E- Grading policy + Weighting (i.e. weight assigned to exams as well as other student work)

Midterm Exam: 30%

Quizzes: 20%

Final Exam: 50%

F- Available university services that support achievement in the course:

N/A

G- Statement on Students with disabilities

Students with Disabilities: Students with disabilities who need special accommodations for this class are encouraged to meet with the instructor and/or their academic advisor as soon as possible. In order to receive accommodations for academic work in this course, students must inform the course instructor and/or their academic advisor, preferably in a written format, about their needs no later than the 4th week of classes.

19. Required equipment:

N/A

20. References:

| A- | Required book (s), assigned reading and audio-visuals: |
|----|--|
| | • Digital Design, M. Mano and Michael D. Ciletti, Pearson, 6th edition, 2017 |
| B- | Recommended books, materials, and media: |
| | • Fundamentals of Logic Design, Charles H. Roth Jr. and Larry L Kinney, Thomson- |
| | Engineering, 7thedition, 2013 |
| | • Digital Fundamentals, Thomas L. Floyd, Prentice Hall; 11 edition, 2014 |

21. Additional information:

Date: -----

Name of Course Coordinator: -----Signature: -----

| Head of curriculum committee/Departme | ent: Signature: |
|---|-----------------|
| Head of Department: | Signature: |
| Head of curriculum committee/Faculty: - | Signature: |
| Dean: | Signature: |

<u>Copy to:</u> Head of Department Assistant Dean for Quality Assurance Course File